

# Simple $\mu$ C acts as dedicated motor control

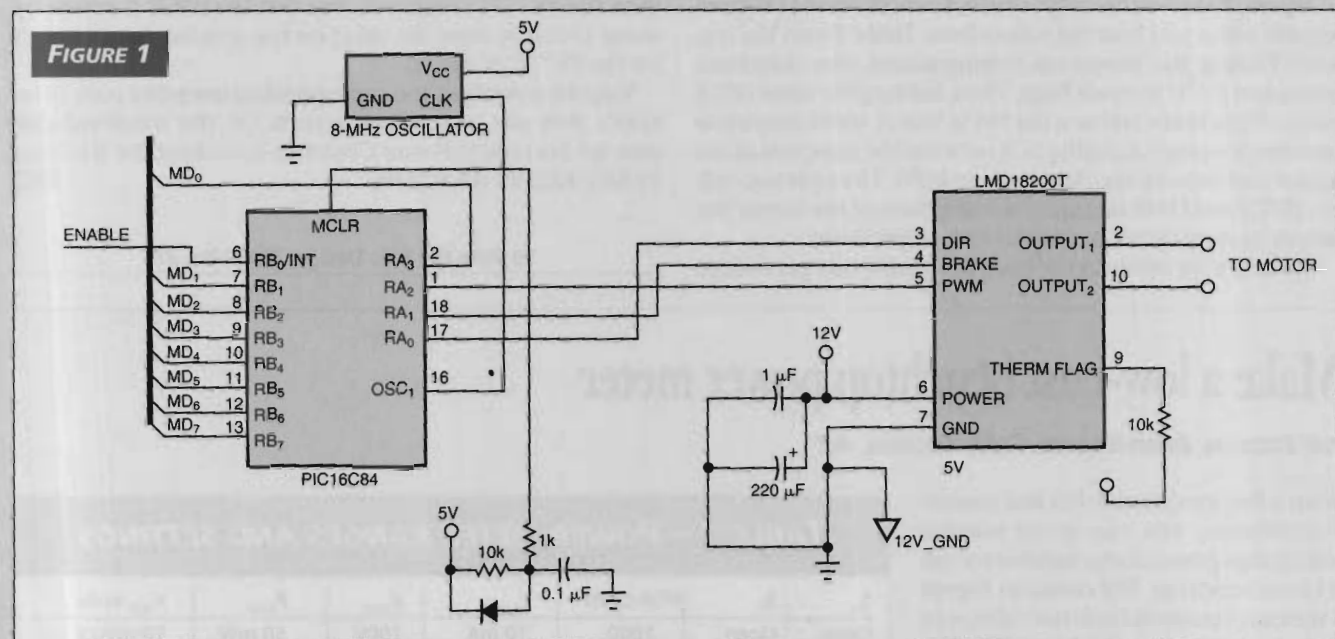
DYLAN HORVATH, GECKO SYSTEMS INC, AUSTIN, TX

Motion-control systems often use a PWM signal to control the duty cycle for a motor driver or amplifier module. Typical designs generate the PWM signals using  $\mu$ Cs with dedicated PWM output lines, such as the PIC16C65 (Microchip Technology, [www.microchip.com](http://www.microchip.com)) and the HC11 (Motorola Inc, [www.motorola.com](http://www.motorola.com)). However, these  $\mu$ Cs may have more features than necessary for a motion-control system with multiple degrees of freedom. Using this type of  $\mu$ C on each degree of freedom becomes costly, particularly if all you need to do is generate motor-control signals.

An alternative approach uses one low-cost  $\mu$ C, in this case the PIC16C84, as a dedicated motor-control register (Figure 1). The circuit accepts control words from an 8-bit digital bus,

and the chip-select line triggers the  $\mu$ C, much the same as other standard 8-bit hardware. You can arrange multiple  $\mu$ Cs on a bus and communicate with a higher level motion-control computer or  $\mu$ C. For example, you can use the parallel port of a PC to control all the degrees of freedom on a robot arm. By using PWM signals to modulate the speed at each joint, coordinated motion is possible.

The  $RA_3$  and  $RB_1$ -to- $RB_7$  data-bus lines are digital inputs that connect to an output-controlled data bus. The PIC16C84 ignores these inputs until there is a high-to-low transition on Pin 6 ( $RB_0/INT$ ). On this transition, the  $\mu$ C places the state of  $RA_3$  on the output  $RA_0$  (direction bit) and places the state of  $RB_1$  on  $RA_1$ . The state of the remaining lines,  $RB_2$  to  $RB_7$ , set



One low-cost  $\mu$ C can operate as a dedicated motor-control register.

TABLE 1—EXAMPLE MOTOR-CONTROL-REGISTER VALUES

| Pulse-width-setting bits |    |    |    |    |    | BRK, DIR |    | HEX  | Description  |
|--------------------------|----|----|----|----|----|----------|----|------|--|
| D7                       | D6 | D5 | D4 | D3 | D2 | D1       | D0 |      |  |
| x                        | X  | x  | x  | x  | X  | 1        | x  | --   | Brake on; motor does not turn                          |
| 1                        | 1  | 1  | 1  | 1  | 1  | 0        | 1  | \$FD | Motor turns clockwise, 100% duty cycle                 |
| 1                        | 1  | 0  | 0  | 1  | 0  | 0        | 0  | \$C8 | Motor turns counterclockwise, $\approx$ 80% duty cycle |
| 0                        | 1  | 1  | 1  | 1  | 1  | 0        | 0  | \$7C | Motor turns counterclockwise, $\approx$ 50% duty cycle |
| 0                        | 1  | 1  | 0  | 0  | 0  | 0        | 0  | \$60 | Motor turns counterclockwise, $\approx$ 20% duty cycle |

the pulse width of the PWM output, RA<sub>2</sub>. Note that these outputs are subject to special conditions.

The RB<sub>0</sub>/INT digital input latches the word on the 8-bit data bus. A 74HC138 1-of-8 device selector drives this active-low input. The high-to-low transition generates an interrupt to update the state of the register. At all other times, the circuit ignores the state of the 8-bit data bus.

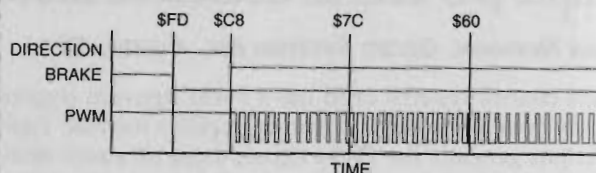
RA<sub>0</sub> drives the motor-drive chip and determines the polarity of the current going through the motor in the output stage of the driver. RA<sub>1</sub> also drives the motor-drive chip. When RA<sub>1</sub> is high and RA<sub>2</sub> is high, active braking of the motor occurs. When RA<sub>1</sub> is high and RA<sub>2</sub> is low, the motor coasts to a stop.

The RA<sub>2</sub> PWM output has a duty cycle that depends on the binary word on the inputs during a high-to-low transition on RB<sub>0</sub>/INT. The duty cycle of this signal increases from 1.56 to 100% in increments of 1.56%. In other words, the duty cycle goes from 1/64 to 64/64 in increments of 1/64, depending on the binary word on RB<sub>2</sub> to RB<sub>7</sub>. The duty cycle repeats at a rate of approximately 300 Hz.

Figure 2 shows the output lines from the motor-control register when you load the values from Table 1 into the register. During the power-up configuration, the direction, brake, and PWM lines are high. Then, loading the value (\$FD) turns off the brake and sets the PWM line at 100% duty cycle (maximum speed). Loading \$C8 switches the direction of the motor and reduces the duty cycle to 80%. The next two values (\$7C) and (\$60) maintain the direction of the motor but reduce its duty cycles to 50% and 20%, respectively.

There is a lag between the time the enable line goes active

FIGURE 2



The output lines of the motor-control register change according to the values of the direction, brake, and PWM signals.

low and the time the  $\mu$ C code can read the value on the data bus. When the enable line triggers an interrupt signal, the  $\mu$ C must save the program counter and the state of its internal registers before the  $\mu$ C can process the interrupt. This delay causes a problem if the value on the data bus changes by the time the PIC  $\mu$ C samples it. You can solve this problem by using a latch to store the value on the data bus long enough for the PIC  $\mu$ C to see it.

You can download the corresponding assembly code from EDN's Web site, [www.ednmag.com](http://www.ednmag.com). (At the registered-user area, go into the Software Center to download the file from DI-SIG, #2239.) (DI #2239)

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## Make a low-cost benchtop power meter

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With a few inexpensive ICs and passive components, you can easily make a multirange power meter suitable for use on your benchtop. The circuit in Figure 1 measures currents from microamps to amps and voltages as high as 100V. The voltage at V<sub>OUT</sub>, which you can monitor with a DVM, indicates the load's power. Two 9V batteries can run the circuit ( $\pm V = \pm 9V$ ), which has a current drain of 10 mA.

The circuit performs an analog multiplication of current and voltage to calculate the power. The load that you want to measure connects between +OUT and -OUT. The supply to the load connects between +IN and -IN. The PGA amplifier (IC<sub>1</sub>) produces a voltage proportional to the load current (I<sub>LOAD</sub>) sensed across R<sub>SENSE</sub>, which sits on the ground side of the supply. R<sub>1</sub>, R<sub>2</sub>, and IC<sub>3D</sub> generate a scaled version of the load voltage equal to V<sub>LOAD</sub>/20. The output of IC<sub>1</sub> and V<sub>LOAD</sub>/20 are the inputs to IC<sub>2</sub>'s precision analog multiplier. IC<sub>2</sub> has a built-in scale factor of 1/10. R<sub>4</sub>, R<sub>5</sub>, and R<sub>6</sub> provide additional gain. A

TABLE 1—POWER METER RANGES AND SETTINGS

| S <sub>0</sub> | S <sub>1</sub> | PGA GAIN | I <sub>MAX</sub>  | V <sub>MAX</sub> | P <sub>MAX</sub> | V <sub>OUT</sub> scale |
|----------------|----------------|----------|-------------------|------------------|------------------|------------------------|
| Open           | Open           | 1000     | 10 mA             | 100V             | 50 mW            | 10 mW/V                |
| Closed         | Open           | 100      | 100 mA            | 100V             | 500 mW           | 100 mW/V               |
| Open           | Closed         | 10       | 1A                | 100V             | 5W               | 1W/V                   |
| Closed         | Closed         | 1        | 10A<br>(see note) | 100V             | 50W              | 10W/V                  |

NOTE: I<sub>MAX</sub> may be lower, depending on the rating of R<sub>SENSE</sub>.

lowpass filter at the output helps reduce noise and provides protection to IC<sub>2</sub> in case V<sub>OUT</sub> accidentally shorts to ground. Combining all the scaling factors gives

$$V_{OUT} = (I_{LOAD} R_{SENSE}) \left( V_{LOAD} \frac{R_2}{R_1 + R_2} \right) PGA_{GAIN} \left( \frac{1}{10} \right) \left( \frac{R_6 + R_4}{R_5} \right) = I_{LOAD} V_{LOAD} \frac{PGA_{GAIN}}{10}$$

The circuit works equally well for positive and negative

load currents and voltages. If the load is producing rather than dissipating power,  $V_{OUT}$  reads negative. The scale of  $V_{OUT}$  is the same for positive and negative power readings. Table 1 shows the ranges.

The maximum load-current setting ( $I_{MAX}$ ) limits the output of  $IC_1$  to 5V to meet head-room requirements when using 9V supplies.  $D_1$  through  $D_5$ ,  $R_3$ , and an LED provide a positive-current-overload warning. When the LED turns on, you should decrease the PGA's gain. A similar string of diodes with opposite polarity can monitor negative-current overloads. Make sure  $R_{SENSE}$  has a sufficient rating to handle the maximum current you use. Also, remember that for high  $I_{LOAD}$ , there is a significant voltage drop across  $R_{SENSE}$ .

The maximum load voltage ( $V_{MAX}$ ) of this circuit is 100V, limiting the voltage at  $IC_2$ 's input to 5V. You can adjust the ratio of  $R_1$  and  $R_2$  for a different  $V_{MAX}$ . Keep the sizes of  $R_1$  and  $R_2$  large to minimize current through them. Their currents add to  $I_{LOAD}$  and cause an error in the power reading.  $IC_{3D}$  prevents  $IC_2$ 's input-bias current from flowing through  $R_1$  and  $R_2$ . The maximum power ( $P_{MAX}$ ) setting limits  $IC_2$ 's output to 5V.

$IC_{3A}$  through  $IC_{3C}$ ,  $IC_{4A}$  and  $IC_{4B}$ , and potentiometers  $R_7$  through  $R_{10}$  provide offset cancellation.  $R_6$  provides gain calibration. The circuit must remove various offsets and gain

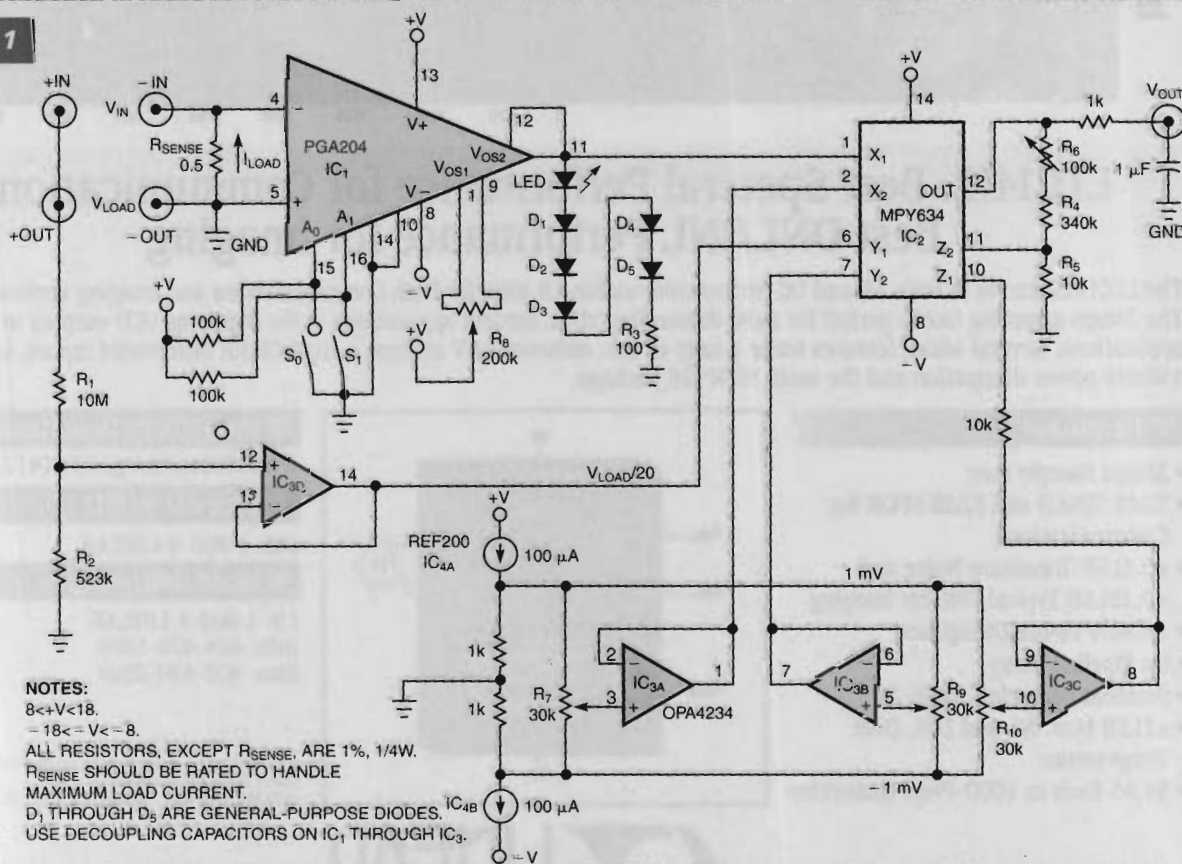
errors to achieve the best accuracy, which is better than 1/2% of full-scale over most of the ranges. If lower accuracy is acceptable, you can remove some or all of the offset cancellation circuitry. To fully calibrate the circuit:

1. Short the load (place a short between +OUT and -OUT) with  $V_{IN}=0$ . Adjust  $R_{10}$  until  $V_{OUT}=0$ , which nulls the offset of the output of  $IC_2$ .
2. Remove the short, set  $PGA=1$ , and apply a large  $V_{IN}$  with no load. Adjust  $R_7$  until  $V_{OUT}=0$ , which nulls the offset of the  $I_{LOAD}$  input to  $IC_2$ .
3. Set  $PGA=1000$  and continue applying  $V_{IN}$  with no load. Adjust  $R_8$  until  $V_{OUT}=0$ , which nulls the offset of the front end of  $IC_1$ . If the PGA gain remains the same,  $R_8$  is unnecessary because  $R_7$  cancels the offset.
4. Short the load. Apply  $V_{IN}$  and increase  $I_{LOAD}$  until the LED starts to turn on. (For  $PGA=1000$ ,  $I_{LOAD}$  is 10 mA to turn on LED.) Adjust  $R_9$  until  $V_{OUT}=0$ , which nulls the offset of the  $V_{LOAD}$  input to  $IC_2$ .
5. Finally, calibrate the gain. Set the  $PGA=100$ , the load=2k, and  $V_{LOAD}=25V$ . Adjust  $R_6$  until  $V_{OUT}$  matches the calculated power. (DI #2250)

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FIGURE 1



A programmable-gain amplifier, an analog multiplier, and a handful of other active and passive components implement a benchtop, multirange power meter.

# Low-battery voltage cutoff consumes just 1 $\mu\text{A}$

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A low-battery voltage-cutoff circuit prevents overdischarge of a rechargeable battery. An obvious requirement of this circuit is extremely low power consumption. Figure 1a's simple circuit has a measured current consumption of approximately 1.2  $\mu\text{A}$  and uses only two components to perform the low-battery cutoff function for a four-NiCd battery.

IC<sub>1</sub> is a 3.9V voltage detector with a maximum hysteresis of 0.3V. When the battery is charged, the 5V power supply exceeds this IC's threshold such that its output goes high to turn on Q<sub>1</sub>, an IRLZ14 MOSFET switch. The IRLZ14 is a logic-level device with an on-resistance of 0.2 $\Omega$ . When the battery voltage drops to below IC<sub>1</sub>'s threshold, the output of IC<sub>1</sub> is zero, which turns off Q<sub>1</sub>.

If the load is heavy, the circuit may turn on and off when the battery voltage reaches the threshold. When the circuit

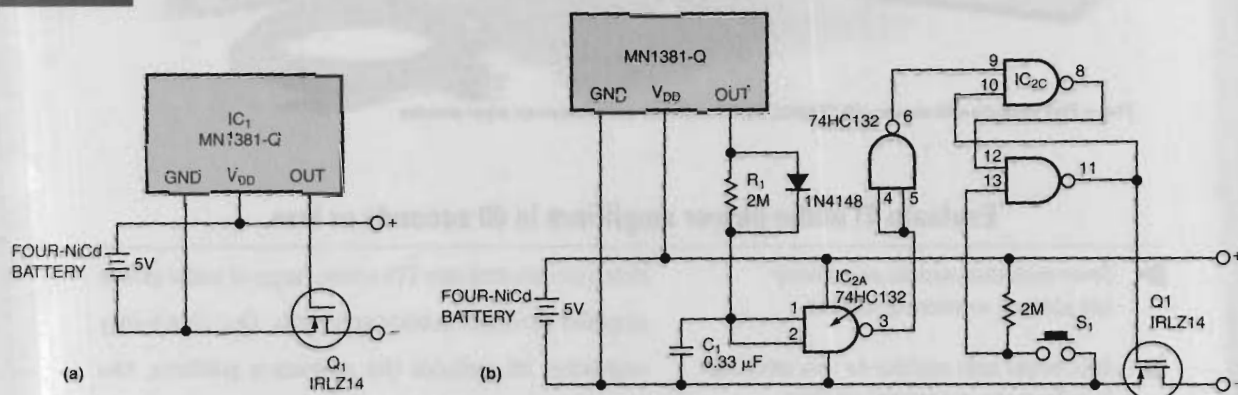
cuts off the load, the battery voltage rises again; this higher voltage may exceed IC<sub>1</sub>'s turn-on threshold. To prevent this problem, the circuit in Figure 1b uses a flip-flop to provide a clean cutoff. Pushing S<sub>1</sub> turns on the switch. When the load has a large capacitance, R<sub>1</sub> and C<sub>1</sub> provide a delayed response to prevent the turn-on in-rush current from triggering the circuit. The power consumption of this circuit is in the same range as that of the circuit pictured in Figure 1a.

All the parts for this idea are available from Digi-Key ([www.digi-key.com](http://www.digi-key.com)). For a lower switch resistance, you can use the IRLZ44, which has an on-resistance of 0.022 $\Omega$ . (DI #2253)

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FIGURE 1



These low-battery-detect circuits cut off when the voltage is lower than 4V and consume approximately 1.2  $\mu\text{A}$ .

# High-voltage circuit breaker protects to 26V

TED SALAZAR, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

Wide use of the Universal Serial Bus (USB) has led to a selection of overcurrent-protection circuits for supply rails of 2.7 to 5.5V, but few products are available for voltages higher than that range. The circuit breaker in Figure 1 operates on supply voltages to 26V and trips at a programmed current threshold.

IC<sub>1</sub> is a high-side current-sense amplifier that monitors supply current via the voltage across R<sub>2</sub> and generates a proportional but smaller current at the OUT terminal as follows:

$$I_{\text{OUT}} = \frac{R_2 \times I_{\text{TRIP}}}{100}$$



$R_1$  and  $R_2$  determine the trip current according to the equation,

$$R_1 = \frac{120}{R_2 \times I_{TRIP}}$$

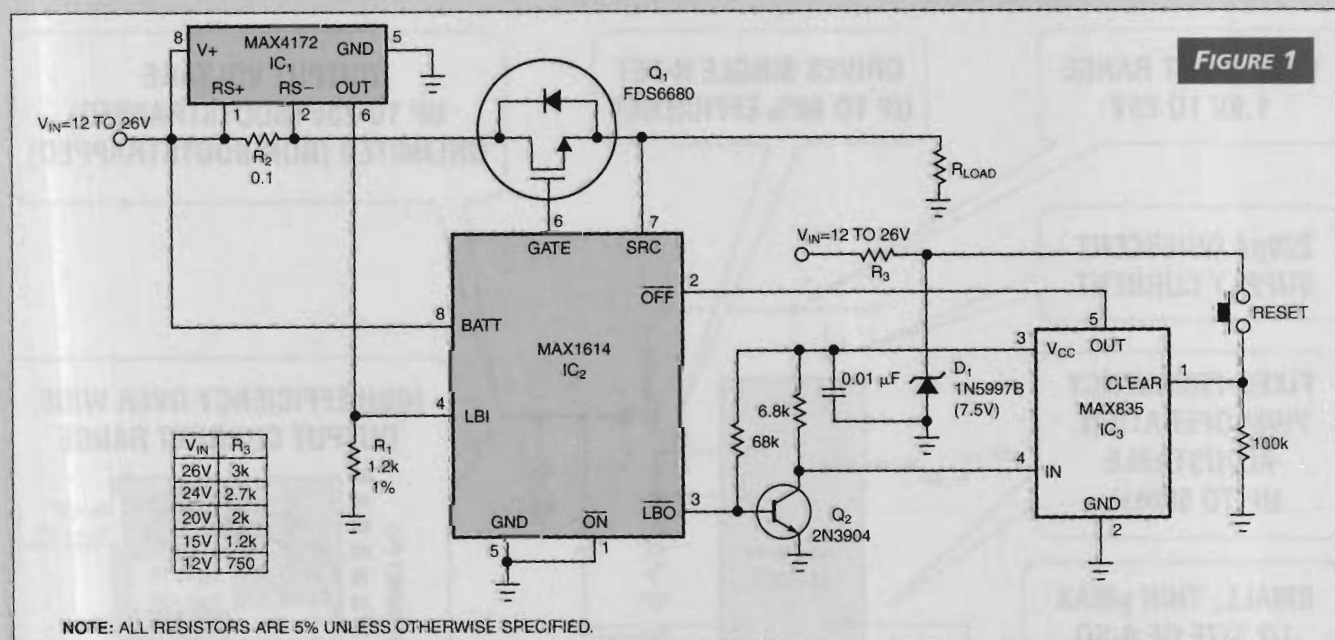
The value of  $R_1$  in Figure 1 sets the trip current at 1A, but values to 10A are acceptable. Supply current at the trip level produces a voltage across  $R_1$  that triggers the low-battery comparator in  $IC_2$ , a high-side, n-channel MOSFET driver. The comparator output ( $\overline{LBO}$ ) drives  $Q_2$  to saturation, causing the latched output of  $IC_3$ , a micropower voltage monitor, to go low. Applied to  $IC_2$ 's Pin 2, this signal disconnects

the power by turning off  $Q_1$ .

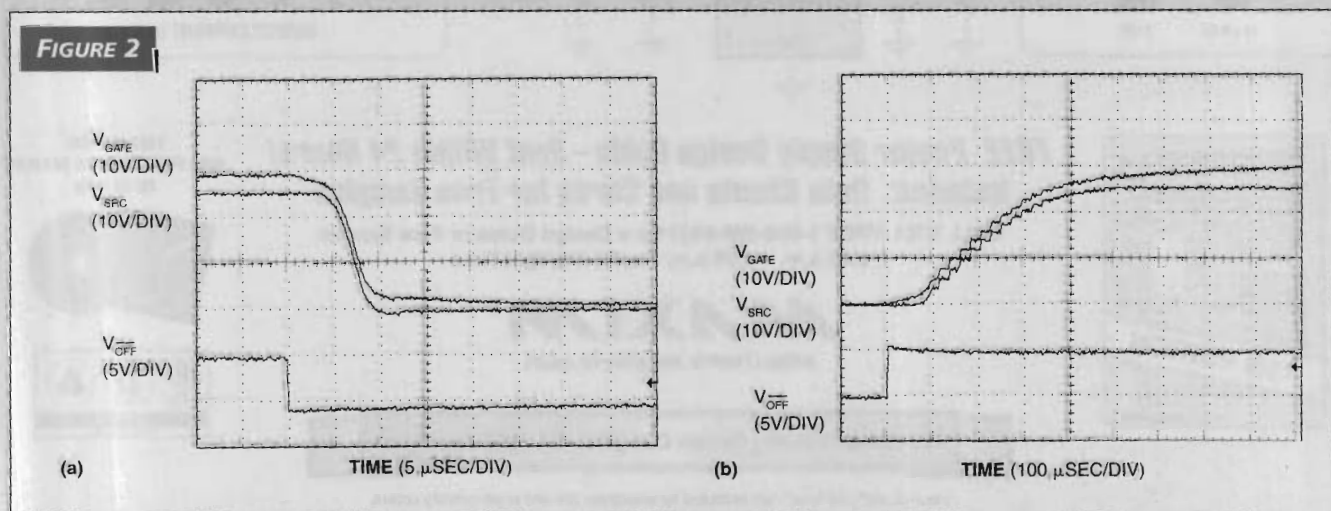
Power remains off until you unlatch  $IC_3$  by depressing the reset button. You may also have to push the button following initial power-up to ensure the correct power-up state. For supply voltages of 12V and higher, choose  $R_3$  according to the table in the Figure 1. For supply voltage that is less than 12V,  $D_1$  and  $R_3$  are unnecessary. The signal delay from  $IC_3$  to the load via  $IC_2$  and  $Q_1$  has a turn-off time of approximately 7  $\mu$ sec (Figure 2a) and a turn-on time of approximately 400  $\mu$ sec (Figure 2b) (DI #2252)

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This circuit provides overcurrent protection for supply-rail voltages to 26V.



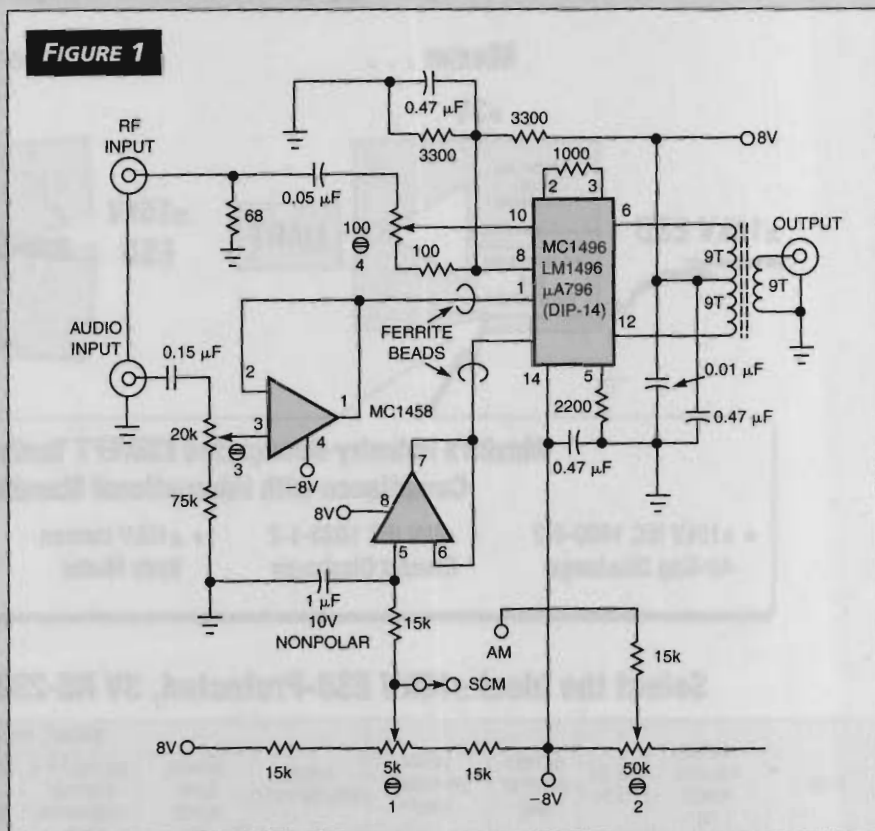
With Figure 1's load-current trip threshold set at 1A, the load voltage  $V_{SRC}$  (middle waveform), turns off (a) and on (b) in approximately 7 and 400  $\mu$ sec, respectively, under the control of the signal at  $IC_2$ 's  $V_{OFF}$  pin.

## Add-on modulator has high bandwidth

**MJ SALVATI, FLUSHING COMMUNICATIONS, FLUSHING, NY**

The simple circuit in **Figure 1** is an add-on modulator that converts the output of a continuous-wave (CW) source to either an amplitude-modulation (AM) or a suppressed-carrier-modulation (SCM) format. Because the circuit has unity gain and 50 $\Omega$  input and output impedances, the CW generator's output-level indications remain valid. The frequency response is flat from 0.3 to 45 MHz and only 0.1 dB down at 0.1 and 60 MHz. The modulation bandwidth is similarly broad: flat to 50 kHz and 3 dB down at 15 Hz with the capacitive coupling shown in **Figure 1**. Modulation levels to 100% are possible. Because the modulation sensitivity is 10% per 100 mV rms of modulating signal, you can read the modulation level directly from the audio generator's output-level indicator.

The circuit is a variation of a standard LM1496/1596 amplitude-modulator setup. It differs from the standard in that it uses a toroidal transformer to provide impedance matching and maximally efficient drive for a low-impedance load, and it drives the modulation ports through unity-gain op amps. The op amp driving Pin 1 provides a high input impedance; thus, it lessens the demands on the audio source and allows practical values for the coupling capacitor. If the audio signal source has no dc component, you can omit the coupling capacitor. You can wind the toroidal transformer with 24-gauge telephone wire over a ferrite core taken from a Sony ([www.sony.com](http://www.sony.com)) 1-421-302 line choke. A Ferronics ([www.ferronics.com](http://www.ferronics.com)) 11-261-J or JW Miller ([www.bellind.com](http://www.bellind.com)) F-50-1 core work equally well. **Figure 1** indicates the adjustment order for the four trim pots. Initially, set all pots to mid-point and inject a 50-mV rms carrier into the RF-input connector. Set the modulation-code switch to SCM and adjust the 5-k $\Omega$  pot for exactly 0V dc at Pin 5 of the MC1458.



**A few trim pots, a toroidal transformer, and a dual op-amp interface with a modulator IC to form a linear, high-bandwidth AM modulator.**

Next, connect an audio signal to the audio-input connector and switch the modulation mode to AM. Adjust both the 50-k $\Omega$  pot and the audio-signal level until you achieve 100% modulation with no peak clipping and no trough overshoot. Once the biasing is set, set the audio generator's output to exactly 500 mV rms then adjust the 20-k $\Omega$  pot for exactly 50% modulation. Last, set the RF input at exactly 50 mV rms and adjust the 100 $\Omega$  pot for 50-mV rms output into a 50 $\Omega$  load. (DI #2245)

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## Simulate signals for telecomm tests

**SAMUEL KEREM, PATTON ELECTRONICS, GAITHERSBURG, MD**

The circuit in **Figure 1** is a miniature gadget that is helpful in telecommunication applications. The function of the device is to simulate data flow with predefined patterns and use these patterns to check a cable's or a receiver's functionality.

The circuit generates a signal in accordance with alternating-mark-inversion (AMI) code. In this type of coding, pulses with alternating polarities represent ones; signals with zero amplitude represent zeros. **Figure 2** shows some examples.

The circuit can produce three AMI-code signal patterns: 1-1-1-1-..., 1-0-1-0-..., and 1-0-0-1-0-0-1-....

The circuit uses a strobe-pulse source, consisting of IC<sub>1A</sub> and IC<sub>1B</sub>. The strobe initiates on the falling edge of the clock only if the previous strobe pulse is over. The strobe-pulse duration is a function of R<sub>1</sub>C<sub>1</sub>. The pulse depends on the state of S<sub>1</sub> and can be nonexistent or close to either 1.5 or 2.5 periods of the clock source (Figure 2b). Therefore, the strobe pulse cuts off at zero, one, or two pulses from the original clock source (Figure 2c). IC<sub>2</sub> divides the modified clock frequency by two and restores the duty cycle to 50%. The signal from IC<sub>2</sub> alternatively switches IC<sub>3</sub>'s internal amplifiers between inverting and noninverting modes with equivalent gain. Thus, IC<sub>3</sub>'s output is a three-level signal.

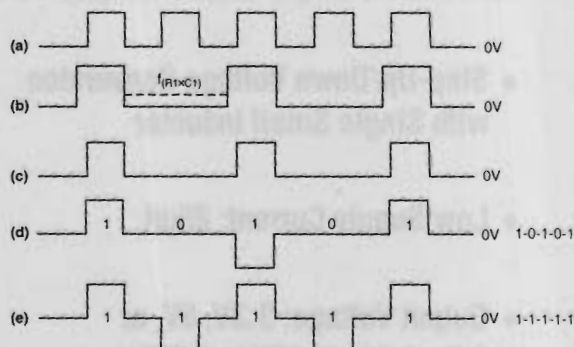
R<sub>2</sub>, C<sub>2</sub>, IC<sub>4A</sub>, and IC<sub>4B</sub> introduce a delay of a few nanoseconds to set the internal amplifiers before the clock signal (Figure 2c) changes at IC<sub>3</sub>'s inputs. R<sub>3</sub> through R<sub>6</sub> set the signal level to the appropriate range. You need IC<sub>5</sub> only if your power supply cannot produce  $\pm 5V$ . You calculate the values of R<sub>1</sub> and C<sub>1</sub> for an 8.448-MHz clock source (E2 bit rate). For

other clock rates, you must recalculate only C<sub>1</sub>'s value. (DI #2247)

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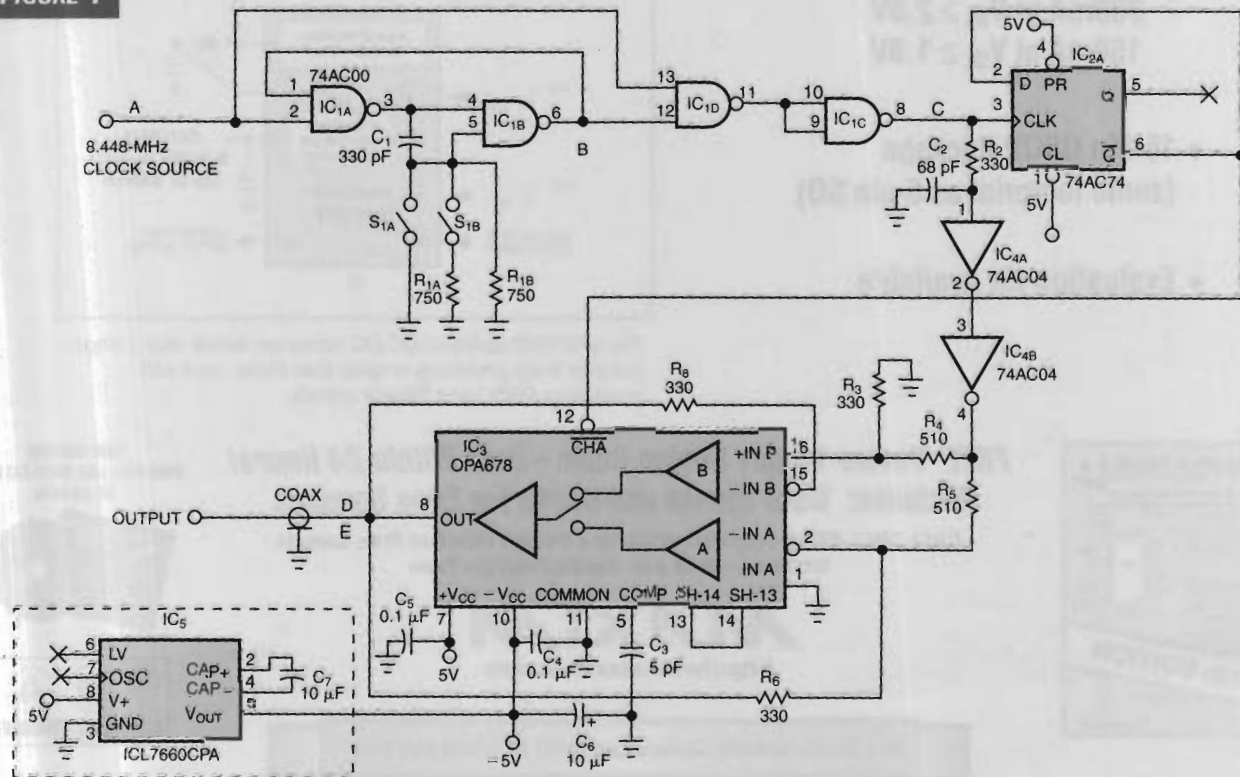
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FIGURE 2



As D and E show, in AMI coding, alternating-polarity pulses denote logic one; no pulse denotes logic zero.

FIGURE 1



A simple bit-pattern generator allows you to test telecommunication equipment.